**Coding-Based Low-Power Through-Silicon-Via Redundancy Schemes for Heterogeneous 3-D SoCs**

Proposed Title

Design and implementation of automated In-built SOC Testing platform with FPGA implementation

Abstract

Three dimensional integration is one of the promising solutions to check the bare 3D integrated circuits before utilizing in the applications. In the existing system design of an heterogeneous architecture is being evaluated using low power silicon redundancy schemes. The technique is based on two optimal coding-based redundancy schemes, used in combination, which allows minimizing the complexity of a redundancy technique in heterogeneous systems. The existing technique reduce the interconnect power consumption. In the proposed system, an automated model of reconfigurable 3D soc testing platform is created in which a design of adjustable SRAM is implemented first. The data in the sram is encoded using Euclidean principle. Further the SRAM is tested with three different test patterns such as Pseudorandom Test, Marching Test and Checker board test. The proposed simulation is executed and verified in MODELSIM / QUARTUS II and implemented partial configuration in XILINX ISE.

**Existing system**

In the existing system design of an heterogeneous architecture is being evaluated using low power silicon redundancy schemes. The technique is based on two optimal coding-based redundancy schemes, used in combination, which allows minimizing the complexity of a redundancy technique in heterogeneous systems. The existing technique reduce the interconnect power consumption.

**Problem Statement**

* Only the interconnects of the existing design SOC is being tested

**Proposed system**

In the proposed system, an automated model of reconfigurable 3D soc testing platform is created in which a design of adjustable SRAM is implemented first. The data in the sram is encoded using Euclidean principle. Further the SRAM is tested with three different test patterns such as Pseudorandom Test, Marching Test and Checker board test. The proposed simulation is executed and verified in MODELSIM / QUARTUS II and implemented partial configuration in XILINX ISE.

**Solution Statement**

* Automated Self Test mechanism is implemented

MODULE DESCRIPTION

**Module 1 Design of Test pattern generation**

Pseudorandom test generation is the simplest method of creating tests. It uses a pseudorandom number generator to generate test vectors, and relies on logic simulation to compute good machine results, and fault simulation to calculate the fault coverage of the generated vectors.

**Module 2 Design of Memory**

This module is used to test the memory using the so called Test methodologies. The test patterns are given into the memory and test validation can be updated.

**Module 3 Design of Memory and Integration**

This module used to integrate the test pattern principles with the Memory module developed.

**BLOCK DIAGRAM**



**SOFTWARE USED**

* XILINX ISE
* MODELSIM 6.3